

WHAT IS CLAIMED IS:

1 1. A method of testing a circuit under design having a
2 plurality of functional elements and having a plurality of clock
3 environments, at least one signal passing from one clock
4 environment to another in said circuit, said method comprising
5 the steps of:

6 modelling at least one of the functional elements to
7 have an unknown state as an output for a predetermined time
8 after a timing event of a clock signal;

9 simulating said circuit; and

10 determining which of said functional elements is a
11 synchroniser to thereby identify if there is a synchronisation
12 problem between for said at least one signal passing from one
13 clock environment to another.

1 2. A method as claimed in claim 1, wherein in the
2 simulation step, a plurality of simulations are carried out with
3 one or more of the following clock signals in said one clock
4 environment and said another clock environment:

5 a) the same clock frequency and phase in said clock
6 environments;

7 b) the same clock frequency and different phase in
8 said clock environments; and

9 c) different clock frequencies in the clock
10 environments.

1 3. A method as claimed in claim 1, wherein in said
2 simulation step, said one clock environment and said another
3 clock environment have the same clock frequency and phase.

1 4. A method as claimed in claim 1, wherein in said
2 simulation step, said one clock environment and said another
3 clock environment have the same clock frequency and a first
4 phase difference.

1 5. A method as claimed in claim 4, wherein said simulation
2 step is repeated with said one clock environment and said other
3 clock environment having the same clock frequency and a second
4 phase difference.

1 6. A method as claimed in claim 5, wherein said second
2 phase difference is of opposite polarity to said first phase
3 difference.

1 7. A method as claimed in claim 1, wherein in said
2 simulation step, said one clock environment and said another
3 clock environment have a different clock frequency.

1 8. A method as claimed in claim 1, wherein said
2 determining step comprises the step of tuning the predetermined
3 time such that an unknown state propagates through only a part
4 of said circuit.

1 9. A method as claimed in claim 1, wherein said
2 determining step comprises using warnings identifying the
3 functional element which is a source of the unknown state and
4 determining if said source has a synchronising function in said
5 circuit.

1 10. A method as claimed in claim 1, wherein the simulation
2 and determining steps are repeated a plurality of times.

1 11. A method of claim 1, wherein said determination step
2 is arranged to identify if a functional element which is a
3 source of said unknown state propagation is a hazard or a
4 synchroniser.

1 12. A method as claimed in claim 1, wherein in said
2 determining step, wherein if a functional element is determined
3 to be a synchroniser, said functional element is arranged such
4 that the unknown state is not propagated.

1 13. A method as claimed in claim 1, wherein if first and
2 second functional elements are identified as first and second
3 synchronisers, said second synchroniser is arranged such that
4 the unknown state is not propagated.

1 14. A method as claimed in claim 1, wherein a first
2 element is identified as a synchroniser, comprising the step of
3 determining the propagation of an unknown state for the
4 remainder of the clock cycle by presence of different values
5 before and after the unknown state presented at an input of the
6 synchroniser.

1 15. A method as claimed in claim 1, wherein said circuit
2 is represented at gate level.

1 16. A method as claimed in claim 1, wherein said circuit
2 is designed in HDL.

1 17. A method as claimed in claim 1, wherein said method is
2 carried out on a simulation tool.

1 18. A method as claimed in claim 1, wherein said timing
2 event comprises a clock edge.

1 19. A method as claimed in claim 1, wherein said
2 functional elements comprise logic gates.

1 20. A method as claimed in claim 19, wherein said logic
2 gates comprise flip-flops.